second input terminal of the second OTA. In a similar vein, claim 17 has been rewritten so as to incorporate the limitations of former claim 16, from which it depended.

Numerous changes have been made to FIGS. 1, 5, 6, 7, 8 and 9 to address the Examiner's objections thereto, and corresponding amendments to the specification have been made. It is believed that the foregoing amendments are sufficient to overcome all of the drawing objections. Corrected formal drawings will be filed upon allowance of the Application.

Likewise, the specification and the claims have been amended in numerous places to address the Examiner's numerous objections and §112 rejections thereto. It is believed that the specification and claim amendments made herein are sufficient to overcome all of the pending objections. No new matter has been entered.

Pursuant to 37 CFR 1.121, marked copies of the amended specification paragraphs and amended claims showing the changes made therein accompany this Amendment.

Turning now to the art rejections, and considering first the rejection of claims 1 and 15 as anticipated by McNeill et al. (U.S. Patent No. 6,150,872), Applicant respectfully submits that this rejection has been made in error. Claims 1 and 15 both require "first and second operational transconductance amplifiers (OTAs)." McNeill et al. does not teach the use of an OTA. Rather, McNeill et al. teaches the use of an operational amplifier, or OP-amp. These are not at all the same. As illustrated in McNeill et al.'s FIG. 1 and described at column 3, lines 12-17, operational amplifiers are devices that directly compare two voltage levels or signals and provide an amplified output voltage signal response based at least in part on the voltage signal comparison. To the contrary, an operational transconductance amplifier receives inputs of

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differential voltages and outputs a current signal. Thus, the symbols used to illustrate these devices are different: a triangle for OP-amp and a trapezoid for OTA. One skilled in the art would recognize that these are not the same elements and are not interchangeable. Since McNeill et al. does not teach the use of two operational transconductance amplifiers, as required by claims 1 and 15, McNeill et al. cannot be said to anticipate these claims, and allowance of claims 1 and 15 is respectfully requested.

With reference now to the rejection of claims 16 and 26 as obvious over McNeill et al., claim 16 requires "first and second operational transconductance amplifiers (OTA)." As argued above with respect to claims 1 and 15, McNeill et al. does not teach the use of an operational transconductance amplifier, but rather, an OP-amp. Moreover, the Examiner's assertion at page 15, line 1 of the Official Action, that "a current is known to be proportional to voltage" is incorrect. Whether a current is proportional to voltage depends, e.g., on the type of conductor. For example, the voltage across a resistor is known to be proportional to the current. However, many cases occur in which the current through a conductor is not directly proportional to the voltage across it, as in the case of nonlinear devices. See Electronic Engineers' Handbook, 3rd Ed., Fink and Christiansen, Editors (1989) at page 1-18 to 1-19, ¶68 (copy attached hereto). Therefore, the rejection of claim 16 as obvious over McNeill et al. is in error and should be withdrawn. Likewise, claim 26 is patentable for the same reasons given above with respect to claim 16, as well as for its own additional limitations. It is therefore respectfully submitted that claims 16 and 26 should be allowed.

Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance.

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A credit card payment Form PTO-2038 authorizing a charge of $336.00 in payment of the added independent claims accompanies this Amendment. In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account Number 08-1391.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on May 20, 2003, at Tucson, Arizona.

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SERIAL NO.: 10/091,776

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MARKED AMENDED SPECIFICATION PARAGRAPHS

Heading at page 1, line 10:

[BACKGRAOUND] BACKGROUND OF THE INVENTION

Paragraph beginning at page 11, line 10:

In accordance with the present invention, the operational amplifier is driven with the constant current, each of two transistors making up an input differential pair has a gate W/L ratio of 1:K2, and the gate W/L ratio of the two transistors forming an active load operating as a load to the two transistors [isK3:1] is K3:1, with offset values being summed together.

Paragraph beginning at page 14, line 9:

An embodiment of the present invention is shown in Fig.1, showing two OTAs (operational transconductance amplifiers) 11 and 12, in which a differential input voltage is proportional to an output current and in which a transconductance exhibits a linear characteristic. Across these OTAs, the current (K2 × gml Δ VBE) having a predetermined constant ratio K2 to an output current (gml Δ VBE) of the first OTA 11, which is proportional to a differential voltage VBE (=VBE2 – VBE1) of the base-to-emitter voltage VBE of two bipolar transistors Q1 and Q2, is caused to flow into the second OTA 12 to produce a voltage corresponding to the differential voltage Δ VBE multiplied by a constant value, that is VPTAT (= K2 × gml Δ VBE/gm2). In the second OTA 12, the base-to-emitter voltage VBE2 of the transistor Q2 is summed to VPTAT and the resulting voltage is output to produce a desired constant voltage VREF not exhibiting a temperature dependent characteristic.

Paragraph bridging pages 16 and 17, beginning at page 16, line 21:

Such a configuration may also be used which includes a source-grounded MOS

transistor MM10, having its drain and gate connected to one end and the other end of the resistor R1, respectively, a source-grounded MOS transistor MM11 having its gate connected to the drain of the MOS transistor [M11] MM10 and a current mirror circuit, having its input end connected to a drain of the MOS transistor MM11, and adapted for supplying the constant current to the MOS transistor MM10, a common source of the first and second MOS transistors MM1 and MM2 of the differential pair, a MOS transistor MM5 of a source follower configuration and to the collector of the bipolar transistor Q1.

Paragraph bridging pages 17 and 18, beginning at page 17, line 7:

Referring to the drawings, certain preferred embodiments of the present invention are explained in detail. Fig.1 shows a circuit configuration of an embodiment of the present invention, as applied to a CMOS reference voltage circuit. As shown in Fig.1, this circuit includes first and second emitter-grounded transistors Q1 and Q2, each of which has a base connected to a collector and is provided with a constant current at the collector, first and second operational transconductance amplifiers (abbreviate to OTAs) 11 and 12, each of which outputs current corresponding to the voltage difference between the voltage at a positive phase(non-inverting) input terminal (+) and that at a reverse phase(inverting) input terminal (-), and a current mirror circuit 13 which has a ratio of the current input to the input end to the current output from the output end equal to a predetermined value K2. The reverse phase input terminal (-) and the positive phase input terminal (+) of the first OTA 11 are connected to the collectors(more precisely the connection nodes of the collectors and the bases) of the first and second transistors Q1 and Q2, respectively. The first OTA 11 has its output terminal connected to an input end of the current mirror circuit 13. An output end of the current mirror circuit 13

and the collector of the second transistor Q2 are connected to the positive phase input terminal (+) and the reverse phase input terminal (-) of the second OTA 12, respectively, while the output terminal of the second OTA 12 is connected to the positive phase input terminal (+) of the second OTA 12. The reference voltage VREF is output at an output terminal of the second OTA 12.

Paragraph beginning at page 18, line 8:

It is assumed that, in the embodiment shown in Fig.1, the emitter area of the transistor Q1 is K1 times the emitter area of the transistor Q2. The collectors of the transistors Q1 and Q2 are connected to drains of the P-channel MOS transistors [M2] M200 and [M3] M300, that is output terminals of a current mirror circuit(made up of P-channel MOS transistors [M1, M2 and M3] M100, M200 and M300) which receives a constant current I0 from a constant current source 14 at its input terminal, and the current I0 flows through collectors of the transistors Q1 and Q2.

Paragraph bridging pages 18 and 19, beginning at page 18, line 17:

If the DC current amplification factor of the transistors is sufficiently close to unity and the base current is neglected, from the above equation (1), the base-to-emitter voltages VBE1 and VBE2 of the transistors Q1 and Q2 are expressed as follows:

$$VBE1=VT\ln\{IC1/(K1\cdot IS)\}$$

$$=VT\ln\{I0/(K1\cdot IS)\} \quad (9)$$

$$VBE2=VT\ln(IC2/IS)$$

$$=VT\ln(I0/IS) \quad (10)$$

Paragraph bridging pages 30 and 31, beginning at page 30, line 14:

Referring to Fig.6, (K2+4) common gate P-channel MOS transistors MP1, MP2 to

MP(K2+4), having respective sources connected to a power supply VDD in common, constitute a first current mirror circuit having (K2+3) outputs. The P-channel MOS transistor MP1, having its drain connected to its gate has the drain connected to a constant current source 16 with a constant current I0 being an input current to the first current mirror circuit. The drains of the P-channel MOS transistors MP2 and MP3 output a constant current to the collectors of the first and second transistors Q1 and Q2, while the drains of the P-channel MOS transistors MP4 to MP(K2+4)[3] output a constant current to the common source of the number 1 to number K2+1 differential pairs. The transistor MN01, having its source grounded, having its drain connected to its gate, having the drain connected to the constant current source IO and fed with the sink current, and the N-channel MOS transistors MN04, MN05 and [MN(K2+1)] MN0(K2+3), having the sources grounded and having the gates to the gate of the transistor MN01 in common, constitute a second current mirror circuit. The transistor MN02, having its source grounded, having its drain connected to its gate, and having the drain connected to the drain of the transistor [MN02] M2, and an N- channel MOS transistor MN03, having its source grounded and having its gate connected to the gate of the transistor MN02 in common, constitute a third current mirror circuit.

Paragraph beginning at page 32, line 1:

The third to number K2 differential pairs are configured in similar manner. The diode-connected transistor M [(2K+2)] (2K2+2) of the number K2+1 last-stage differential pair has its drain connected to the drain of the output transistor MN03 of the third current mirror circuit, and is driven by the current proportional to that flowing in the transistor M2 of the first differential pair.

Paragraph beginning at page 32, line 8:

The first differential pair(made up of transistors M1 and M2) is driven by the transistor MP4 with a current Io proportional to the constant current I0. If a differential voltage Δ VBE is differentially input to the first differential pair, and the drain currents flowing through the transistors M1 and M2 of the first differential pair are I1 and I2, we have

I1 + I2 = Io.

The common source of the transistors [MP (2K+1) and MP(2K2+2)] M (2K2+1) and M (2K2+2) of the last-stage number (K2+1) differential pair is fed with the current Io from the transistor MP(K2+4), the drain of the transistor M(2K2+2) is driven by the transistor MN03 with the current I2, with the current Io – I2 = I1 flowing through the drain of the transistor M(2K2+1). The differential input voltage of the number (K2+1) is Δ VBE, with the gate voltage of the transistor M(2K2+1) being lower by Δ VBE than the gate voltage of the transistor M(2K2+2).

Paragraph bridging pages 35 and 36, beginning at page 35, line 1:

The differential pair made up of P-channel MOS transistors M1 and M2 receives a differential voltage of output voltages of the transistors Q1 and Q2. An output voltage of the transistor Q2 is applied to the gate of the P-channel MOS transistor M3 making up a second differential pair along with the diode-connected P-channel MOS transistor M4. The drain of the transistor M4 is driven with a current proportional to an output current of the first differential pair, that is the drain current of the transistor M2 (K3 tuple current). The common source of the first and second differential pairs is driven with two constant currents, having a certain current ratio to each other. A desired amplification factor is realized by setting the operating input voltage range of the second differential pair so as to be a preset constant number tuple of that of

the first differential pair. In Fig.7, P-channel MOS transistors [M5 to M9] MP5 to MP9, which have their sources connected in common to a power supply VDD and have their gates connected in common, constitute a first current mirror circuit. The P-channel MOS transistor [M9] MP9, having its drain connected to its gate has the drain connected to a constant current source 17, with the constant current I0 being an input current to the current mirror circuit. From the drains of the P-channel MOS transistors [M5 and M7] MP5 and MP7, constant currents are fed to the collectors of the first and second transistors Q1 and Q2, and from the drains of the P-channel MOS transistors [M6 and M8] MP6 and MP8, constant currents are fed to the commonly connected sources of the first and second differential pairs respectively. An N-channel MOS transistor MN10, having a source grounded, having a drain and a gate connected to each other and having the drain connected to the drain of the transistor M2, and an N-channel MOS transistor MN11, having a source grounded and having a gate connected to the gate of the transistor MN10, constitute a second current mirror circuit.

Paragraph beginning at page 37, line 1:

The sources of the transistors M1 and M2 are connected to the drain of the P-channel MOS transistor [M6] MP6, forming an output of the first current mirror circuit. From the conditions for the driving current,

$$I_{D1} + I_{D2} = I_0 \qquad (23)$$

Paragraph bridging pages 41 and 42, beginning at page 41, line 7:

In Fig.8, transistors MM1 to MM7 constitute a voltage follower type operational amplifier with a resistance for compensation RC and a capacity for compensation CC. The W/L ratio of input differential transistors MM1 and MM2 is set to 1:K2, and the W/L ratio of

active load transistors MM3, and MM4, operating as loads, is set to K3:1, so that input offset is produced. The transistors MM1 and MM2, having sources connected in common to a drain of the constant current source transistor [M5] MM6, form a differential pair. The transistor MM3, connected to the drain of [the current source] transistor MM1, and having its source grounded, and the transistor MM4, having its drain connected to the drain of the transistor MM2, having its source grounded and having its gate connected to the gate of the transistor MM3, form a current mirror circuit operating as a load for the differential pair. The drain of the transistor MM2, forming an output of the differential pair,[has its source grounded, while having its drain] is connected to the gate of the transistor M5, the drain of which is connected to a drain of the constant current source transistor MM7. An output voltage VREF is taken at a drain of the transistor MM5, operating as an output terminal. The output terminal is connected to the gate of the transistor MM2 that operates as an inverting input terminal of the differential pair. A resistor RC for phase compensation and a capacity CC are connected across the drain and the gate of the transistor MM5. A base-to-emitter voltage VBE of the transistor Q1 is input to a non-inverting input terminal of the differential pair.

Paragraph beginning at page 42, line 10:

The drain currents ID1 and ID2 of the respective transistors MM1 and MM2 are given by:

$$I_{D1} = \beta (V_{GS1} - V_{TH})^2 \qquad (33)$$

$$I_{D2} = K3\, \beta (V_{GS2} - V_{TH})^2 \qquad (34)$$

The following relationship holds:

$$I_{D1} + I_{D2} = I_0 \qquad (35)$$

Paragraph beginning at page 42, line 20:

Moreover, from the conditions of the active load transistors MM3 and MM4, we have

$$K3I_{D1} = I_{D2} \quad (37)$$

Solving the equations (35) and (37),

$$I_{D1} = I_0 K3/(K3+1) \quad (38)$$

$$I_{D2} = I_0/(K3+1) \quad (39).$$

Paragraph beginning at page 44, line 5:

A circuit comprised of a transistor MM10, having a source grounded, a drain connected to one end of a resistor R1 and having a gate connected to the opposite end of the resistor R1, a transistor MM11, having a source grounded and having a gate connected to the drain of the transistor MM10, and the resistor R1, makes up a Nagata current mirror circuit. Here, with the transistors MM13 and MM12 forming a current source, the transistors MM10 and MM11 and the resistor R1 form a self-biased Nagata current mirror circuit.

Paragraph beginning at page 44, line 14:

Here, the transistor MM10 is assumed to be a unit transistor, and the ratio of the gate width W to gate length L, or (W/L), of the transistor MM11, is assumed to be K1 times that of the unit transistor, where $K1 > 1$.

Paragraph beginning at page 44, line 18:

In the MOS Nagata current mirror circuit, shown in Fig.8, the device is assumed to exhibit satisfactory matching, the channel length modulation and the substrate effect are neglected, and the relationship between the drain current and the gate-to-source voltage of the MOS transistor is assumed to follow the square rule. Then, the drain current ID1 of the MOS

transistor MM10 is given by:

$$I_{D1} = \beta (V_{GS10} - V_{TH})^2 \qquad (42).$$

Paragraph beginning at page 45, line 1:

The drain current ID2 of the MOS transistor MM11 is given by:

$$I_{D2} = K1\ \beta (V_{GS11} - V_{TH})^2 \qquad (43)$$

There is also the following relationship:

$$V_{GS10} = V_{GS11} + R1 I_{D10} \qquad (44).$$

Paragraph beginning at page 46, line 2:

It is noted that transistors [M15 and M14] MM11 and MM10 make up a current mirror circuit, while the transistors [M15 and M14] MM13 and MM14 drive MM10 and MM11, respectively. Thus, the transistors [M15 and M14] MM11 and MM10 make up a MOS self-biased Nagata reference current circuit, with

$$I_{D10} = I_{D11} \qquad (46)$$

Thus,

$$\Delta V_{GS} = V_{GS10} - V_{GS11} = R_1 I_{D10} \qquad (47)$$

Solving the equation (39) from the equation (37),

[0149]

$$I_{D10} = I_{D11} = \frac{1}{R_1^2 \beta}\left(1 - \frac{1}{\sqrt{K_1}}\right)^2 \qquad (48)$$

Paragraph beginning at page 47, line 7:

Also, the transistor MM12 forms a current mirror circuit with the transistor MM13, so that

$I_{D12}=I_{D13}$ (51).

Paragraph beginning at page 50, line 8:

Since the circuit of the present embodiment takes the configuration of a voltage follower type operational amplifier, it is possible to subtract the offset voltage. In this case, the connection of various circuit components may be kept unchanged as shown in Fig.8 and only the gate W/L ratio of the transistors MM1 and MM2 and the gate W/L ratio of the transistors MM3 and MM4 are changed to K2:1 and to 1:K3, respectively. The output voltage VREF of the reference voltage circuit in this case is given by:

VREF=VBE1-VOS (57).

Paragraph beginning at page 51, line 2:

Fig.9 shows a modification of the embodiment shown in Fig.8. The drain and the gate of the transistor MM2 of the differential pair are connected together and the output VREF is taken out from the drain. In Fig.9, the output voltage VREF of the reference voltage circuit is given by:

$VREF=VBE+V_{OS}$,

as in equation (54), where V_{OS} is given by the equation (53).

That is, a reference voltage not dependent upon temperature is output, as mentioned above. Although this modification lacks in capability of feeding a current from the reference voltage output terminal, it is effective as a voltage source for supplying the reference voltage.

Paragraph beginning at page 52, line 10:

The reason is that, in the reference voltage circuit of the present invention, the circuitry is constructed [measly by] merely using active devices, without employing resistors as in the conventional circuitry shown in Fig.10.

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MARKED AMENDED CLAIMS

2. (Amended) [The CMOS reference voltage circuit as defined in claim 1] A CMOS reference voltage circuit for generating and outputting a reference voltage, including:

first and second diode-connected transistors, respectively grounded and driven by two constant currents with a constant current ratio; and

means for amplifying a differential voltage between output voltages of said first and second diode-connected transistors by a predetermined factor and summing a resulting amplified voltage to the output voltage of said first or second diode-connected transistor, in which

said means for amplifying and summing comprises:

first and second operational transconductance amplifiers (OTAs); and

a current mirror circuit, wherein

said first OTA has an output terminal and receives said differential voltage; and

said second OTA has a first input terminal for receiving the output voltage from said first or second diode-connected transistor and has a second input terminal connected to an output terminal of said second OTA and driven with a current proportional to an output current of said first OTA, an output terminal voltage of said second OTA being said reference voltage;

said current mirror circuit having an input end connected to the output terminal of the first OTA and an output end connected to the second input terminal of the second OTA,

wherein the transconductance gm1 of said first OTA is equal to the transconductance gm2 of said second OTA (gm1 = gm2); and

the current ratio of an input current to an output current in said current mirror circuit being set to 1:K2, where K2 > 1, to attain a desired amplification factor.

3. (Amended) [The CMOS reference voltage circuit as defined in claim 1] A CMOS reference voltage circuit for generating and outputting a reference voltage, including:

first and second diode-connected transistors, respectively grounded and driven by two constant currents with a constant current ratio; and

means for amplifying a differential voltage between output voltages of said first and second diode-connected transistors by a predetermined factor and summing a resulting amplified voltage to the output voltage of said first or second diode-connected transistor, in which

said means for amplifying and summing comprises:

first and second operational transconductance amplifiers (OTAs); and

a current mirror circuit, wherein

said first OTA has an output terminal and receives said differential voltage; and

said second OTA has a first input terminal for receiving the output voltage from said first or second diode-connected transistor and has a second input terminal connected to an output terminal of said second OTA and driven with a current proportional to an output current of said first OTA, an output terminal voltage of said second OTA being said reference voltage;

said current mirror circuit having an input end connected to the output terminal of the first OTA and an output end connected to the second input terminal of the second OTA,

wherein the current ratio of an input current to an output current in said current mirror circuit is 1:1; and

wherein the transconductance gm1 of said first OTA1 and [that] the transconductance gm2 of said second OTA 2 are set so that

$gm1 = K2 \times gm2$, where $K2 > 1$

to attain a desired amplification factor.

4. (Amended) [The CMOS reference voltage circuit as defined in claim 1] A CMOS reference voltage circuit for generating and outputting a reference voltage, including:

first and second diode-connected transistors, respectively grounded and driven by two constant currents with a constant current ratio; and

means for amplifying a differential voltage between output voltages of said first and second diode-connected transistors by a predetermined factor and summing a resulting amplified voltage to the output voltage of said first or second diode-connected transistor, in which

said means for amplifying and summing comprises:

first and second operational transconductance amplifiers (OTAs); and

a current mirror circuit, wherein

said first OTA has an output terminal and receives said differential voltage; and

said second OTA has a first input terminal for receiving the output voltage from said first or second diode-connected transistor and has a second input terminal connected to an output terminal of said second OTA and driven with a current proportional to an output current of said first OTA, an output terminal voltage of said second OTA being said reference voltage;

said current mirror circuit having an input end connected to the output terminal of the first OTA and an output end connected to the second input terminal of the second OTA,

wherein the current ratio of an input current to an output current in said current mirror circuit is set to 1:K2, where $K2 > 1$; and

wherein the transconductance gm1 of said first OTA1 and the transconductance gm2 of said second OTA 2 are set so that

$gm1 = K3 \times gm2$, where $K3 > 1$

to attain a desired amplification factor.

5. (Amended) A CMOS reference voltage circuit for generating and outputting a reference voltage, including:

first and second diode-connected transistors, respectively grounded and driven by two constant currents with a constant current ratio; and

means for amplifying a differential voltage between output voltages of said first and second diode-connected transistors by a predetermined factor and summing a resulting amplified voltage to [an] the output voltage of said first or second diode-connected transistor, in which

said means for amplifying and summing comprises (K2+1) differential pairs, K2 being an integer [not less] greater than 1, wherein

the first differential pair receives said differential voltage;

one [of differential pair transistors] transistor of the second differential pair receives [an] the output voltage of the first or second diode-connected transistor, whilst the other transistor of said second differential pair [transistors] is diode-connected and is driven with a current proportional to an output current of one of the transistors of the first differential pair;

output voltages of diode-connected transistors of the second to number K2 differential pairs are applied to one of the differential pair transistors of the third to the number (K2+1) differential pairs, respectively, whilst the other transistors of the differential pair transistors are diode-connected and driven by currents proportional to the output current of the one transistor of the first differential pair;

the first to number (K2+1) differential pairs are driven with the (K2+1) constant

currents bearing a predetermined constant current ratio relative to one another; and

the differential input voltages of the second to number (K2+1) differential pairs are summed together to produce an amplified voltage with a desired amplification factor.

6. (Amended) A CMOS reference voltage circuit for generating and outputting a reference voltage, including:

first and second diode-connected transistors, respectively grounded and driven by two constant currents with a constant current ratio; and

means for amplifying a differential voltage between output voltages of said first and second diode-connected transistors by a predetermined factor and summing a resulting amplified voltage to [an] the output voltage of said first or second diode-connected transistor, in which

said means for amplifying and summing comprises (K2+1) differential pairs, K2 being an integer greater than 1, wherein

the first differential pair receives said differential voltage;

one [of differential pair transistors] transistor of the second differential pair receives [an] the output voltage of the first or second diode-connected transistor, whilst the other transistor of said second differential [transistors] is diode-connected;

the differential transistors of the third to number K2 differential pairs are diode-connected, a diode-connected differential transistor of a preceding stage and a diode-connected differential transistor of a subsequent stage being driven by constant currents with a predetermined constant current ratio K2;

the differential transistors of the number (K2+1) differential pairs are diode-connected, one diode-connected differential transistor being driven by a constant current along with the

other diode-connected differential transistor of a preceding stage, the other diode-connected transistor being driven with the current proportional to the output current of said first differential pair;

the first to number (K2+1) differential pairs are driven with (K2+1) constant currents bearing a certain constant current ratio to one another; and

the differential input voltages of the second to number (K2+1) differential pairs are summed together to produce a desired amplification factor.

7. (Amended) A CMOS reference voltage circuit for generating and outputting a reference voltage, including:

first and second diode-connected transistors, respectively grounded and driven by two constant currents with a constant current ratio; and

means for amplifying a differential voltage between output voltages of said first and second diode-connected transistors by a predetermined factor and summing a resulting amplified voltage to [an] the output voltage of said first or second diode-connected transistor, in which

said means for amplifying and summing is comprised of two differential pairs,

one of the differential transistors of a second one of said differential pairs receiving [an] the output voltage of the first or second diode-connected transistors, the other differential transistor being diode-connected and being driven with a current proportional to an output current of one of the transistors of the first differential pair;

said first differential pair and the second differential pair being driven with two constant currents having a constant current ratio to each other;

an operating input voltage range of said second differential pair being a predetermined

number multiple of the operating input voltage range of said first differential pair to produce a desired amplification factor.

8. (Amended) The CMOS reference voltage circuit as defined in claim 7 wherein the emitter area of said first diode-connected transistor is equal to the emitter area of said second diode-connected transistor, with the ratio of two constant currents corresponding to said first and second diode-connected transistors not being equal to 1.

9. (Amended) The CMOS reference voltage circuit as defined in [claims] claim 7 wherein the size of the first diode-connected transistor is K1 times the size of the second diode-connected transistor, with the driving current ratio of said first and second diode-connected transistors not being equal to 1,

wherein K1 is an integer greater than 1.

10. (Amended) The CMOS reference voltage circuit as defined in claim 7 wherein the size of the first diode-connected transistor differs from the size of the second diode-connected transistor, with the driving current ratio of said first and second diode-connected transistors being equal to 1.

11. (Amended) The CMOS reference voltage circuit as defined in claim 7 further comprising a third differential pair, wherein the gate W/L ratio of each transistor of said first differential pair is K2 times the gate W/L ratio of each transistor of said second differential pair, W and L being the gate width and the gate length of the transistor, respectively;

the driving current of said second differential pair being K3 times the driving current of said third differential pair; the output current of the first differential pair being multiplied by K3 to drive the diode-connected transistor of the second differential pair to produce the desired

amplification factor;

wherein K2 and K3 are integers greater than 1.

17. [The reference voltage circuit as defined in claim 16] A reference voltage circuit, comprising:

first and second emitter-grounded bipolar transistors, each having a base connected to a collector, with each collector being fed with a respective constant current;

first and second operational conductance amplifiers (OTAs), each having at least a first input terminal and a second input terminal and adapted for outputting from an output terminal a current proportional to a differential voltage between voltages applied to said first and second input terminals; and

a current mirror circuit having at least an input end and an output end, with the ratio of the current fed to said input end to the current output from the output end being of a predetermined value, wherein

the collectors of the first and second bipolar transistors are connected respectively to the first and second input terminals of the first OTA;

said output terminal of said first OTA is connected to said input end of said current mirror circuit;

the output terminal of said second OTA and said collector of said second bipolar transistor are respectively connected to the first and second input terminals of said second OTA; and

a connection node of said first input terminal and the output terminal of said second OTA are connected to said output end of said current mirror circuit, said output terminal of said

second OTA outputting a reference voltage; wherein

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor is of a value different from 1 and the [same] respective constant [current is] currents are equal and are supplied to the respective collectors;

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor being of a value equal to 1 and the ratio of the respective constant currents driving the first bipolar transistor and the second bipolar transistor being of a value different from 1; or

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor being of a value different from 1 and the ratio of the respective constant currents driving the first bipolar transistor and the second bipolar transistor being of a value different from 1; and

the differential voltage Δ VBE of the base-to-emitter voltages (VBE1 and VBE2, respectively) of said first and second bipolar transistors being of a value proportional to VT (thermal voltage) having a positive temperature characteristic;

the current ratio of said current mirror circuit being K2;

the values of transconductance of said first and second OTAs being gm1 and gm2, respectively; and

the reference voltage output from said output end of said second OTA being given by

$VBE2 + \{K2 \times \Delta VBE[2] \times gm1\}/gm2$.

18. (Amended) A reference voltage circuit comprising:

first and second bipolar transistors, each having a emitter grounded and having a base

connected to a collector, with each collector being fed with a respective constant current;

a first differential pair comprised of a pair of MOS transistors, having sources connected in common and driven with a single constant current and having gates for receiving differentially base-to-emitter voltages of said first and second bipolar transistors;

a current mirror circuit having an input end and plural(K2) number of output ends, said current mirror circuit receiving from said input end an output current of said first differential pair and outputting output currents proportional to the input current at said plural (K2) number of output ends;

a second differential pair comprised of a pair of MOS transistors, having sources connected in common and driven with a single constant current, one of the MOS transistors having a gate fed with [a] the base-to-emitter voltage of said second bipolar transistor and the other MOS transistor having a gate connected to a drain and connected to the first output end of said current mirror circuit; and

third to number (K2+1) differential pairs, each comprised of a pair of MOS transistors, having sources connected in common and driven with a single constant current, one MOS transistor of said differential pair of said third to number (K2 + 1) differential pairs having a gate connected to a gate of a MOS transistor of a preceding stage differential pair having a drain connected to a gate, the other MOS transistor of said differential pair having a drain connected to a gate and connected to a corresponding output end of the current mirror circuit;

a reference voltage being taken out at [a] the drain of the other MOS transistor of the number (K2+1) differential pair having the drain and the gate connected together.

19. (Amended) A reference voltage circuit comprising:

first and second bipolar transistors, each having a emitter grounded and having a base connected to a collector, with each collector being fed with a respective constant current;

a first differential pair comprised of a pair of MOS transistors, having sources connected in common driven with a single constant current and having gates for receiving differentially base-to-emitter voltages of said first and second bipolar transistors;

a first current mirror circuit having an input end and an output end, said first current mirror circuit receiving from said input end an output current of said first differential pair and outputting output currents proportional to the input current at said output end;

a second current mirror circuit having an input end and plural(K2) number of output ends, said second current mirror circuit receiving from said input end a constant current from a constant current source and outputting output currents proportional to the input constant current at said K2 output ends;

a second differential pair comprised of a pair of MOS transistors, having sources connected in common driven with a single constant current, one of the MOS transistors having a gate fed with [a] the base-to-emitter voltage of said second bipolar transistor and the other MOS transistor having a gate connected to a drain and connected to the first output end of said second current mirror circuit;

third to number K2 differential pairs, each comprised of a pair of MOS transistors, having sources connected in common driven with a single constant current, each MOS transistor having a drain and a gate connected together, one MOS transistor of said differential pair of said third to number (K2 + 1) differential pairs, having a drain connected to a drain of the other MOS transistor of a preceding stage differential pair, said other MOS transistor having a drain and a

gate connected together, said drain of said one MOS transistor being connected to the corresponding output end of the second current mirror circuit,

the other MOS transistor of said differential pair, having a drain connected to a drain of one MOS transistor of a subsequent stage differential pair, said one MOS transistor having a drain and a gate connected together, said drain of the other MOS transistor being connected to a corresponding output end of said second current mirror circuit; and

a number [(K2+1)] (2K2+1) differential pair[, each comprised of] comprising a pair of MOS transistors[,] having sources connected in common driven with a single constant current, each MOS transistor of said pair having a drain and a gate connected together, the drain of one of the MOS transistors being connected to the drain of the other MOS transistor of the number K2 differential pair having a drain and a gate connected together, said drain being connected to said output end of said first current mirror circuit, a reference voltage being taken out at the drain of the other MOS transistor as an output terminal.

20. (Amended) The reference voltage circuit as defined in claim 18 wherein

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor is of a value different from 1 and the [same] respective constant [current is] currents are equal and are supplied to the respective collectors;

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor is of a value equal to 1 and the ratio of the respective constant currents driving the first bipolar transistor and the second bipolar transistor is of a value different from 1; or

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor is of a value different from 1 and the ratio of the respective constant currents

bipolar transistor is of a value different from 1 and the ratio of the respective constant currents driving the first bipolar transistor and the second bipolar transistor is of a value different from 1; and wherein

the differential voltage Δ VBE of the base-to-emitter voltages (VBE1 and VBE2, respectively) of said first and second bipolar transistors is of a value proportional to VT (thermal voltage) having a positive temperature characteristic;

the reference voltage output from said number [K2] (K2 + 1) differential pair being given by VBE2 + K2 $\times$ Δ VBE[2].

21. A reference voltage circuit comprising:

first and second bipolar transistors, each having a emitter grounded and having a base connected to a collector, with each collector being fed with a respective constant current;

a first differential pair comprised of a pair of MOS transistors, having sources connected in common driven with a single constant current and having gates for receiving differentially base-to-emitter voltages of said first and second bipolar transistors;

a current mirror circuit having an input end and an output end, said input end being fed with an output current of said first differential pair and said output end outputting an output current corresponding to a preset proportion of the input current; and

a second differential pair comprised of a pair of MOS transistors, having sources connected in common driven with a single constant current, the gate of one of the MOS transistors being fed with [a] the base-to-emitter voltage of said second bipolar transistor, the other MOS transistor having a drain and a gate connected together and connected to said output end of said current mirror circuit;

a reference voltage being taken out from the drain of the other MOS transistor of said second differential pair as an output terminal.

27. (Amended) The reference voltage circuit as defined in claim 19 wherein

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor is of a value different from 1 and the [same] respective constant [current is] currents are equal and are supplied to the respective collectors;

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor is of a value equal to 1 and the ratio of the respective constant currents driving the first bipolar transistor and the second bipolar transistor is of a value different from 1; or

the ratio of the emitter area of the first bipolar transistor to the emitter area of the second bipolar transistor is of a value different from 1 and the ratio of the respective constant currents driving the first bipolar transistor and the second bipolar transistor is of a value different from 1; and wherein

the differential voltage Δ VBE of the base-to-emitter voltages (VBE1 and VBE2, respectively) of said first and second bipolar transistors is of a value proportional to VT (thermal voltage) having a positive temperature characteristic;

the reference voltage output from said number [K2] (K2 + 1) differential pair being given by VBE2 + K2 $\times$ Δ VBE[2].

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FIG . 1

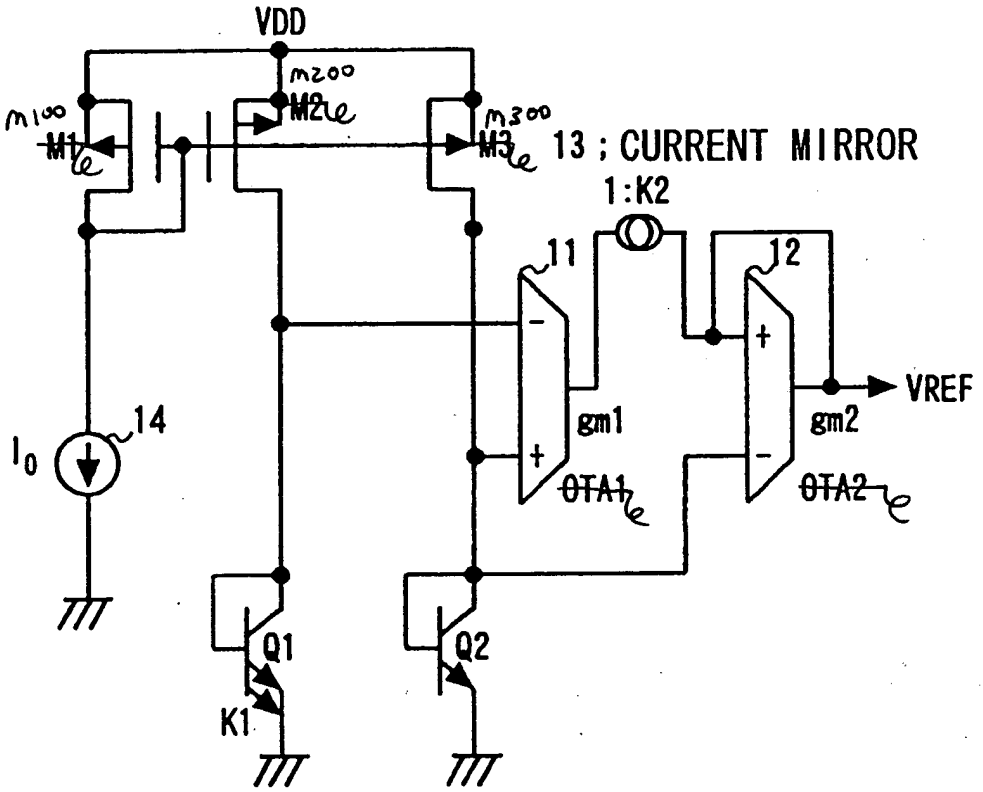
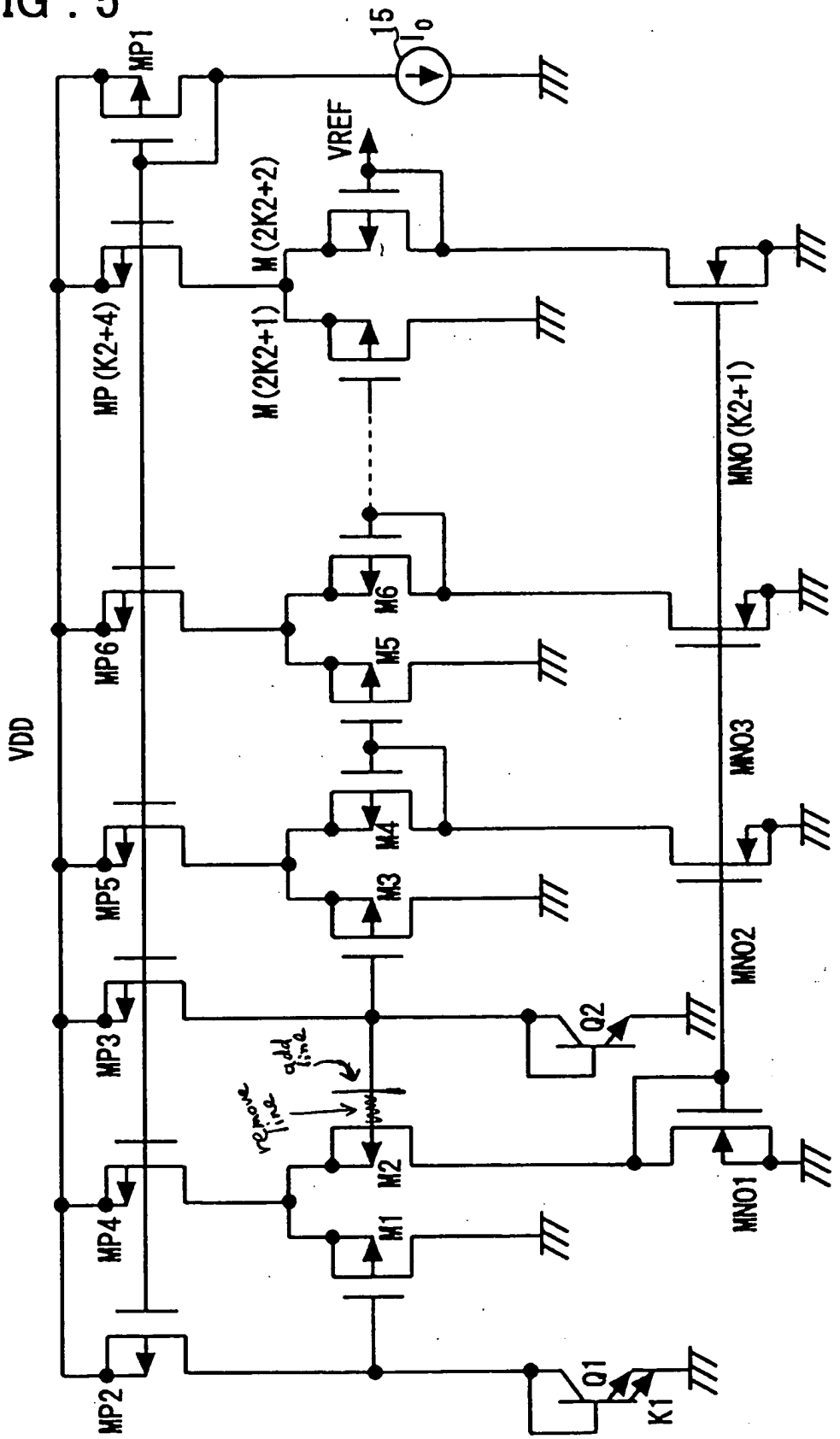


FIG . 5



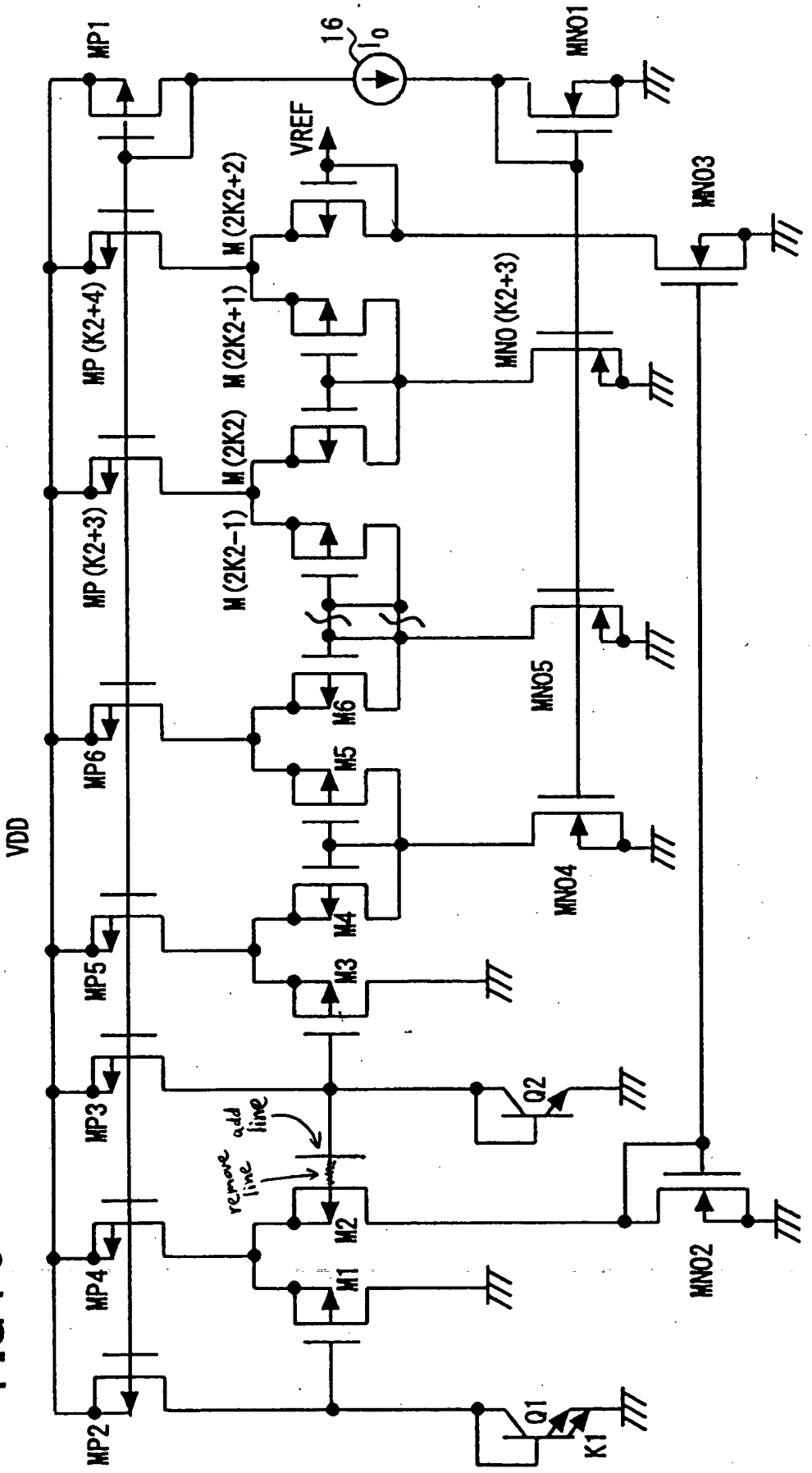
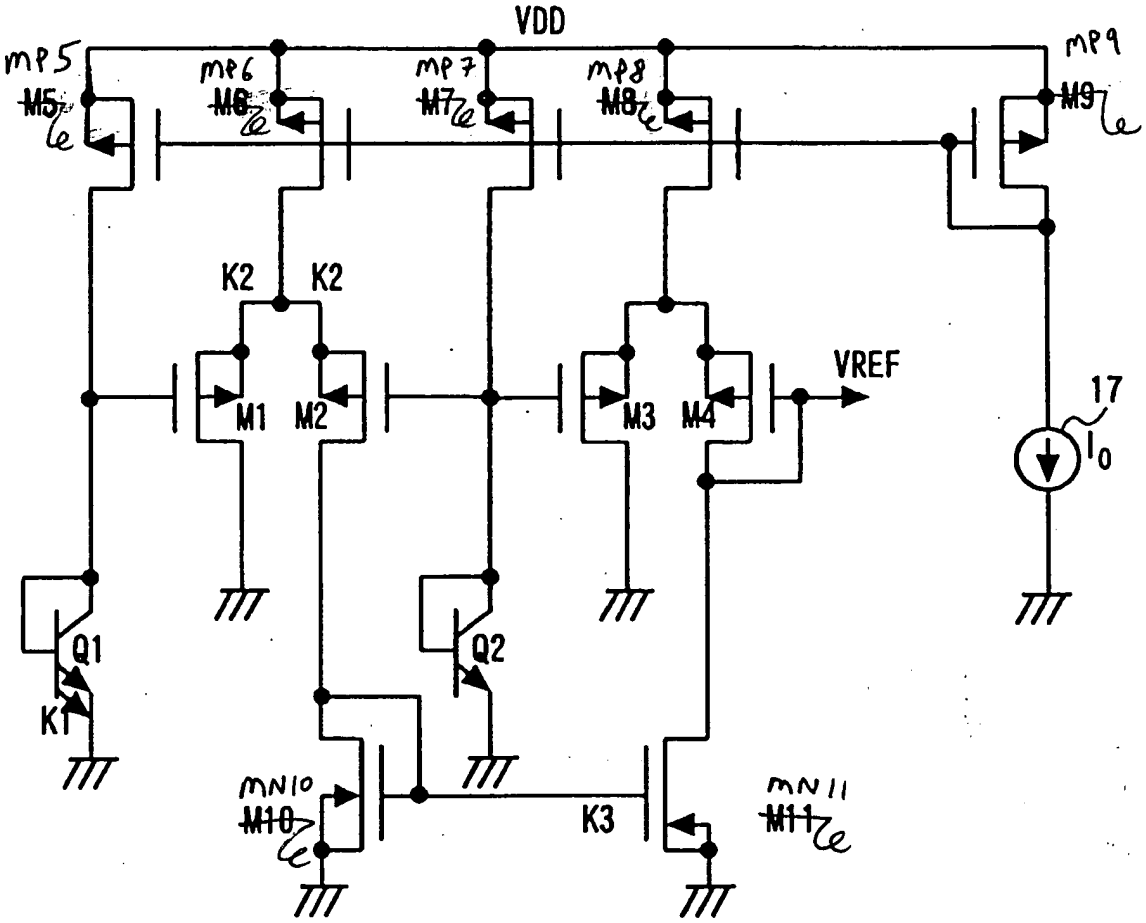


FIG. 6

FIG . 7



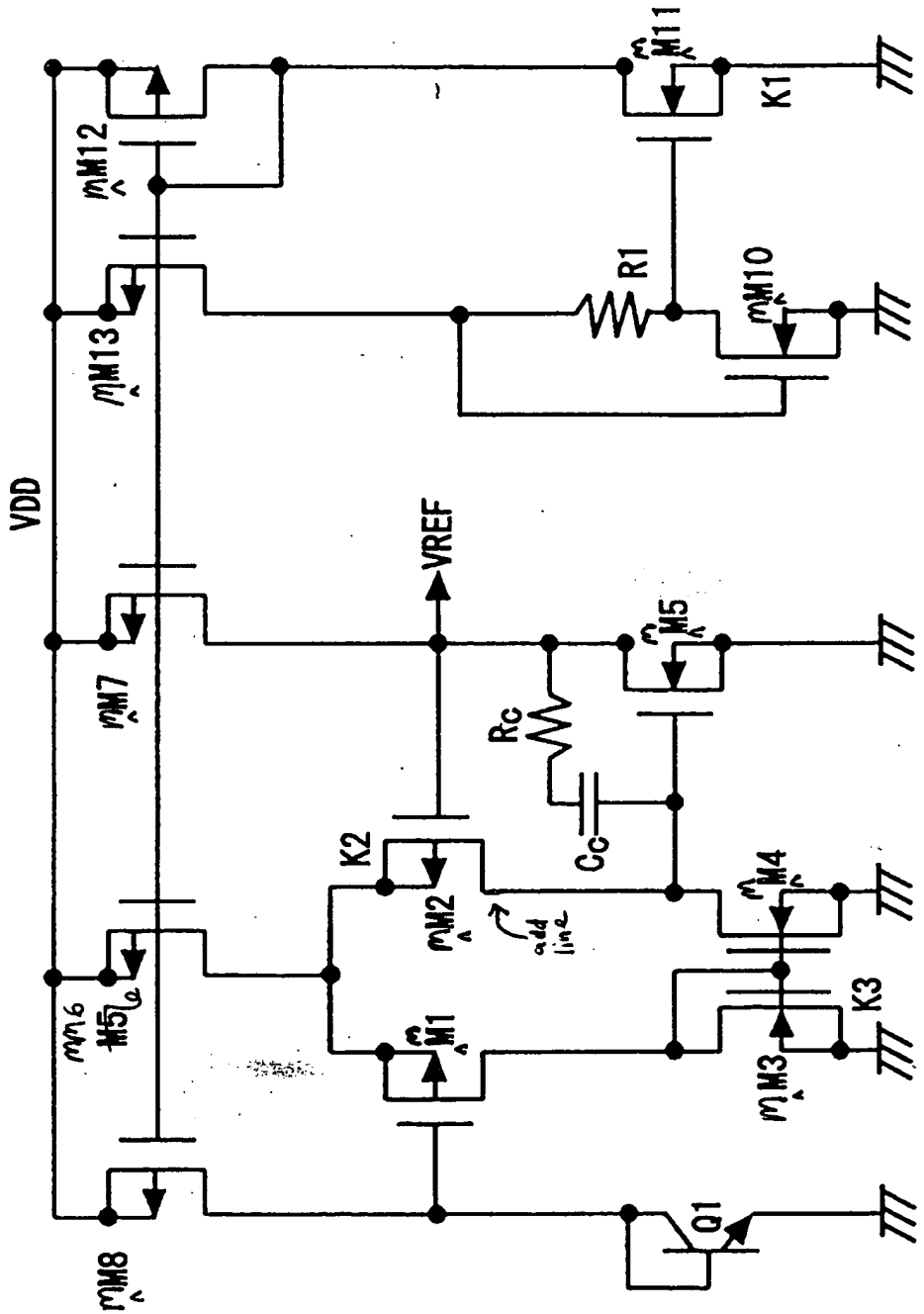


FIG. 8

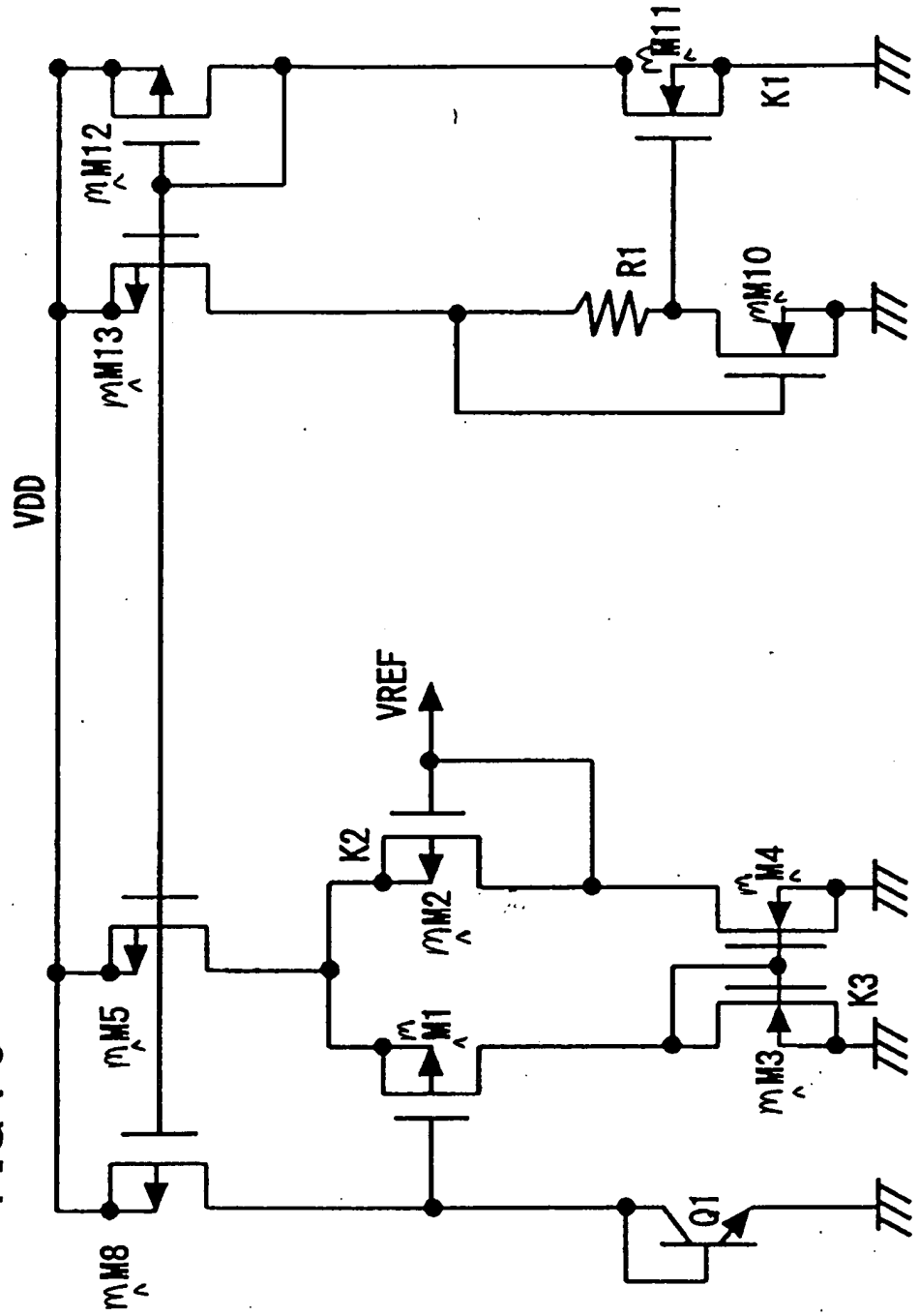


FIG. 9